

**IN THE SPECIFICATION**

Amend the specification by inserting, before the first line:

--This is a continuation application of U.S. Serial No. 09,928,413, filed August 14, 2001; which is a continuation application of U.S. Serial No. 09/525,011, filed March 14, 2000, now U.S. Patent No. 6,295,045; which is a continuation application of U.S. Serial No. 09/294,432, filed April 20, 1999, now U.S. Patent No. 6,121,947; which is a continuation application of U.S. Serial No. 08/770,373, filed November 29, 1996, now U.S. Patent No. 5,909,205. This application is also related to U.S. Serial No. 09/500,237, filed February 8, 2000, now U.S. Patent No. 6,219,020, and U.S. Serial No. 08/891,751, filed July 14, 1997, now U.S. Patent No. 6,088,014.--.

Pages 3 and 4, the paragraph bridging these pages from page 3, line 19, to page 4, line 2, replace the bridging paragraph with:

The control signal RDCT comprises a read clock signal SRCK, a read reset signal RSTR, a write clock signal WCK, a reset write signal RSTWN, a read clock signal RCK, a reset read signal RSTRN and a data selection signal SELDT. Of these signals, the read clock signal SRCK and the read reset signal RSTR are supplied to the field memory 1201. The write clock

signal WCK, the reset write signal RSTWN, the read clock signal RCK~~RCD~~ and the reset read signal RSTRN are supplied to the line buffer 1202 of the frame memory circuit 1106. The data selection signal SELDT are supplied to the read-out data select circuit 1203 of the frame memory 1106.

Page 4, the first full paragraph (lines 3-6), replace the paragraph with:

The read-out data select circuit 1203 selects any one of an output data D1 of the field memory 1201 and an output data D2 of the line buffer 1202, and outputs the selected data as frame memory read-out data Dout~~data~~.

Page 4, second full paragraph (lines 7-10), replace the paragraph with:

On the basis of the data Dout~~data~~, the frame memory read-out and display data generating circuit 1107 as described above generates serial liquid crystal display data which are compatible with the liquid crystal display unit 1110.

Page 25, the paragraph containing Table 3, replace the paragraph with:

TABLE 3

INPUT MODE	CONVERSION RATE	SIZE AFTER CONVERSION
640*350	2→3	960*525
640*400	2→3	960*600
640*480	2→3	960*720
800*600	4→5	1000*750
1024*768	THOUGH <u>THROUGH</u>	1024*768

Page 27, third full paragraph (lines 14-17), replace the paragraph with:

The input video signal activating circuit 204 activates ~~activate~~ the frame memory write control circuit 214 at a predetermined timing which is determined on the basis of the synchronous signal (VSYNC-N/HSYNC-N) 103 and the dot clock 106.

Page 30, first full paragraph (lines 9-13), replace the paragraph with:

Likewise, the line memory write control circuit 216 generates a line memory write control signal (clock : LWCLK / write reset : LRSTW-N). The line memory read control circuit 217 generates a line memory read control clock signal (clock :

LRCLK / write reset : LRSTR-N). The line memory write control signal and the line memory read control signal constitute the line memory control signal 114 in Fig. 1.